Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1, 4, and 7-11 have been canceled. Claims 3, 5, 6, and 13 have been amended to be written in independent form. Also, claim 13 has been amended to correct a typographical error. Dependent claims 2 and 12 have been amended to depend from amended independent claims 6 and 13, respectively. In addition, dependent claim 12 has been amended to correct antecedent basis.

New claims 14-27 have been added. Support for new claims 14, 15, 18, 21, and 25 is found, *inter alia*, in originally filed independent claim 7. Support for new claims 16 and 19 is found, *inter alia*, in originally filed claim 2. Support for new claims 17 and 20 is found, *inter alia*, in originally filed claim 10. Support for new independent claim 22 is found, *inter alia*, in originally filed claims 1, 2, 3, and 6, and in the specification on page 15, lines 9-11, page 18, lines 9-12, and page 21, lines 15-17. Support for new claims 23, 24, and 27 is found, *inter alia*, in originally filed claims 5, 6, and 13, respectively. Support for new claim 26 is found, *inter alia*, in originally filed claim 8. No new matter has been added.

Listing of Claims:

Claims 1 (canceled)

Claim 2 (amended): The ~~multi-chip module~~ instrument controller of claim [[1]]6, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog.

Claim 3 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 1, wherein~~comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for ~~re~~routing signals within the ~~multi-chip~~ instrument controller.

Claim 4 (canceled)

Claim 5 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 1, further~~ comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor;

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor; and

a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

Claim 6 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 5,~~comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claims 7-11 (canceled)

Claim 12 (amended): The method for conducting multiple parallel ~~monitoring and control functions~~processing using a single ~~multi-chip module~~ instrument controller as in claim [[11]]13, further comprising the additional step of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations.

Claim 13 (amended): [[The]]A method for conducting multiple parallel ~~monitoring and control functions~~processing using a single ~~multi-chip module~~ instrument controller ~~as in claim 11, further comprising the step of~~having a processor and a field programmable array, the method comprising:

receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths (thereby generating digital inputs);

providing a first portion of the digital inputs to the processor;

providing a remaining portion of the digital inputs to the field programmable gate array;

performing digital signal processing on the first portion of the digital inputs utilizing the processor;

receiving the remaining portion of the digital inputs at the field programmable gate array and configuring a first portion of the gates in the field programmable gate array to perform digital signal processing on the remaining portion of the digital inputs, thereby conducting multiple parallel processing using a single instrument controller; and

configuring a ~~section~~second portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claim 14 (new): The instrument controller according of claim 3, wherein a third portion of the gates in the field programmable gate array is configured to activate the instrument controller from a deactivated state, or to deactivate the instrument controller from an active state.

Claim 15 (new): The instrument controller of claim 3, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 16 (new): The instrument controller of claim 3, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

Claim 17 (new): The instrument controller of claim 3, wherein a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claim 18 (new): The instrument controller of claim 5, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 19 (new): The instrument controller of claim 5, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

Claim 20 (new): The instrument controller of claim 5, wherein a portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claim 21 (new): The instrument controller of claim 6, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 22 (new): A stand-alone instrument controller comprising:

a plurality of gates arranged in a field programmable gate array having multiple portions of gates, the multiple portions of gates including:

a first portion of the gates in the field programmable gate array is configured to perform signal processing,

a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, and

a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter;

a microprocessor coupled to the plurality of gates, and configured to operate independently or under the control of the plurality of gates;

a non-volatile memory storage system with non-volatile storage components for programs and data storage coupled to both the microprocessor and the plurality of gates;

a large volatile memory storage system coupled to the microprocessor with volatile storage components having a memory size that is comparable to, or larger than, an address space operated upon by the microprocesser;

a plurality of analog-to-digital converters for receiving a plurality of analog inputs and digitizing the analog inputs, thereby providing digital inputs for use in the instrument controller; and

a plurality of analog outputs where each analog output is controlled by an independent digital-to-analog converter, and each independent digital-to-analog converter is configured to convert from one of at least two possible depths to analog.

Claim 23 (new): The stand-alone instrument controller of claim 22, further comprising a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

Claim 24 (new): The stand-alone instrument controller of claim 22, wherein the internal embedded power converter is configured to receive an input voltage level and to generate each operating and reference voltage needed within the instrument controller.

Claim 25 (new): The stand-alone instrument controller of claim 22, wherein the microprocessor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 26 (new): The stand-alone instrument controller of claim 22, further comprising at least two internal oscillators coupled to the microprocessor for providing clock signals for low-frequency and high-frequency operations.

Claim 27 (new): A method for conducting multiple parallel processing using a single instrument controller having a field programmable array, the method comprising:

> configuring a portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving at least one input voltage level and generating each operating and reference voltage needed for activation, operation, and deactivation of the instrument controller.